AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-10 (Cancelled)

11. (New) A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs, wherein

each of the match line pairs has a precharge circuit;

the precharge circuit drives the first match line of the match line pair to the first voltage and the second match line thereof to the second voltage lower than the first voltage, respectively;

each of the memory cells has a storage circuit and a comparator;

each of the comparators has the first and the second MOS transistors;

gate electrodes of the first and second MOS transistors are connected to the search lines, respectively;

either of source or drain electrodes of the first and second MOS transistors are connected to the first match line; and

the second match line is put in a floating state when comparison operation is performed in the comparator.

12. (New) The semiconductor integrated circuit device according to claim 11, wherein

a source - drain path in the first MOS transistor is included in the first current path between the first and the second match lines;

a source - drain path in the second MOS transistor is included in the second current path between the first and the second match lines;

the comparator generates a signal voltage corresponding to a result of comparing data stored at the storage circuit and data inputted via the search lines at the match line.

13. (New) The semiconductor integrated circuit device according to claim 12, wherein

the first and the second coupling capacitances being parasitic between the search line and the first match line

are larger than the third and the fourth coupling capacitances being parasitic between the search line and the second match line.

14. (New) The semiconductor integrated circuit device according to claim 13, wherein

a match detector is arranged in each of the second match lines; and

the match detector determines the data-comparison result by discriminating voltages of the second match line.

15. (New) The semiconductor integrated circuit device according to claim 14, wherein

the storage circuit has two transistors and two capacitors.

16. (New) A semiconductor integrated circuit device comprising a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs, wherein

the match line pair has a precharge circuit;

the precharge circuit drives the first match line of the match line pair to the first voltage and the second match line thereof to the second voltage lower than the first voltage, respectively;

the memory cell has a storage circuit and a comparator;

the comparator comprises

the first and the second MOS transistors connected serially so as to form the first current path between the first and the second match lines, and

the third and the fourth MOS transistors connected serially so as to form the second current path;

gate electrodes of the first and third MOS transistors are connected to the search lines, respectively;

either of electrodes of source or drain electrodes of the first and the third MOS transistors are connected to the first match lines through contacts formed through self-aligned process;

gate electrodes of the second and fourth MOS transistors are connected to the storage circuits, respectively; and

either of electrodes of source or drain electrodes of the second and fourth MOS transistors are connected to the second match lines through contacts formed through self-aligning process.

17. (New) The semiconductor integrated circuit device according to claim 16, wherein

the first and the second coupling capacitances being parasitic between the search lines and the first match lines are generated principally by the contacts, respectively;

the third and the fourth coupling capacitances being parasitic between the search lines and the second match lines are generated principally by an interlayer insulator formed between a first metal layer used for forming the plurality of the search line pairs and a second metal layer used for forming the plurality of the second match lines; and

the first and the second coupling capacitances are larger than the third and the fourth coupling capacitances, respectively.

18. (New) A semiconductor integrated circuit device comprising a plurality of the first match lines, a plurality of search line pairs intersecting the plurality of the first match lines, a plurality of bit line pairs paralleling to the plurality of search line pairs, and a plurality of memory cells arranged at intersecting points of the

plurality of the first match lines with the plurality of search line pairs, wherein

the memory cell has a storage circuit and a comparator;

the storage circuit is connected to one of the bit line pairs;

the comparator is connected to one of the search line pairs and one of the first match lines;

the voltage amplitude of the plurality of bit line pairs is larger than that of the plurality of search line pairs;

a plurality of second match lines parallel to the plurality of first match lines are provided;

a plurality of match line pairs formed in a paired manner by the plurality of first match lines and the plurality of second match lines have precharge circuits, the plurality of precharge circuits drive the first match lines of the match line pairs to a first voltage and the second match lines of the match line pairs to a second voltage lower than the first voltage, respectively, and the comparator is inserted between the plurality of match line pairs to compare data held at the storage circuit and data inputted via the plurality of search lines; and

the second match line is put in a floating state at a time of comparison operation in the comparator.

19. (New) The semiconductor integrated circuit device according to claim 18, wherein

each of the storage circuits has two transistors and two capacitors.